Amendments to the Specification:

Please replace the paragraph found on page 25, lines 6-24 with the following amended paragraph:

One possible implementation of a transmitter circuit suitable for use in the present bus interface is shown in FIG. 13, which depicts an exemplary 2-bit embodiment that includes transmitters Tx0 and Tx1. The modulators 250, 252 are preferably implemented with exclusive-OR gates, the outputs of which ($cd0(t)=D0(t)\oplus C0(t)$ and $cd1(t)=D1(t)\oplus C1(t)$) are routed through multiplexers 254 and 256 to output drivers 262 and 264. The multiplexers and output drivers are preferably clocked with the dual edge of the DLL clock (clk/clkb for even/odd data~~, where 'even' data is ??? and odd data is ???~~) derived from system clock 208; this provides a data rate of 2 Gb/s/pin for a 1 GHz DLL clock. The driver outputs are connected together at an I/O pad 266 to produce the 3-level output signal coupled to data channel 200. The output drivers preferably have a current-mode open-drain structure. The spread data, cd0(t) and cd1(t), occupy twice the bandwidth of the base-band data, and thus the bandwidth expansion factor of 2 makes the timing margin weaker.